Fabrication and Characterization of Pseudo-MOSFETs

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1 Introduction

Microelectronics has undergone an enormous development in recent years with an ever increasing performance of integrated circuits. This development has been made possible by modern CMOS technology, notably the down-scaling of transistor dimensions that leads to an exponentially increasing number of transistors on a chip, known as the famous Moor’s law. Figure 1 shows a schematics of a conventional n-type bulk-Si MOSFET consisting of highly n-type doped source and drain areas within a p-type substrate. In addition, a MOSFET features a gate electrode of length \( L \) and width \( W \) that is insulated from the bulk-Si substrate by an insulator (typically SiO\(_2\)) of thickness \( d_{ox} \). The two p-n-junctions will prevent current flow from source to drain. Applying a gate voltage \( V_{gs} \) across an insulating gate oxide at the channel, the carrier concentration at the channel/gate interface can be controlled from accumulating the channel majority carriers through depleting free carriers to accumulation of channel minority carriers (inversion). In the case of inversion, current can flow from source to drain. The saturation current through a MOSFET is to first order given by the following expression:

\[
I_d \approx \mu_{eff} \frac{W}{L} C_{ox} \frac{(V_{gs} - V_{th})^2}{2}
\]

where \( C_{ox} = \varepsilon_{ox} / d_{ox} \) is the geometrical oxide capacitance per unit area, \( \mu_{eff} \) is the effective carrier mobility and \( V_{gs,th} \) are the gate and threshold voltages, respectively. Obviously, a higher current (which translates into a faster performing integrated circuit) is obtained when the channel \( L \) length is scaled down and/or the effective carrier mobility is increased. In the past, a performance increase of MOSFET devices has almost exclusively been obtained by (down-)scaling the transistor dimensions. However, in the very near future continuing the down-scaling will become difficult due to a number of issues. One of the major obstacles is related to the appearance of so-called short channel effects (SCE), i.e. a loss of electrostatic gate control over the potential in the channel region. Short channel effects arise due to an overlap of the source-channel and channel-drain p-n-junctions yielding a strongly reduced potential barrier as illustrated in Fig. 1 (b). SCE are deleterious since they lead to drastically increased off-state leakage currents and thus to an enormous increase of power consumption of highly integrated circuits. Therefore, the semiconductor industry - notably AMD and IBM - have replaced the traditional bulk-Si substrates with silicon-on-insulator (SOI) technology. SOI substrates consist of a thin silicon layer of thickness \( d_{SOI} \) on top of a so-called buried oxide (BOX) of thickness \( d_{box} \). A major benefit of SOI is that short channel effects can be suppressed effectively by scaling down the SOI-layer thickness \( d_{SOI} \) enabling a more drastic down-scaling of the channel length than possible with bulk-Si technology. If at the same time the effective carrier mobility could be increased, a strongly improved device performance is obtained. Recently, strain-silicon has been introduced as a “new” silicon material with up to 100% in-
creased mobility. In particular, strained silicon-on-insulator has attracted a great deal of interest since it allows combining scalability and transistor improvements due to the higher mobility. However, when fabricating the appropriate strained-SOI substrates it is indispensable to constantly measure the carrier mobility in a field-effect transistor device. This requirement calls for a fast turn-around device characterization method. To this end so-called Pseudo-MOSFETs are fabricated for extraction of the carrier mobility which will be explained in detail below. In the present lab-training, such Pseudo-MOSFET devices with different contacting schemes will be fabricated, measured and characterized.

Figure 1: (a) Schematics of a conventional bulk-Si MOSFET. (b) Illustration of the appearance of short channel effects in a scaled device: the white line represents the conduction band along current transport direction in a long-channel device. In a device suffering from SCE, the source-channel and channel-drain p-n-junctions overlap leading to a lowering of the potential barrier in the channel (green solid line). As a result, devices exhibiting SCE show an exponentially increased off-state leakage leading to a drastic increase of power consumption and eventually a loss of the ability to switch the device.

2 The pseudo-MOSFET

In SOI substrates the active silicon layer is separated from a silicon handle wafer by a (rather thick) oxide, called the buried oxide (BOX). Therefore the idea of the pseudo-MOSFET is to use this buried oxide as the actual gate oxide and the silicon handle wafer as the gate electrode. In this case, only source and drain contacts have to be defined in order to realize a MOSFET structure. Hence, the pseudo-MOSFET concept allows a quick and straight forwards realization of MOSFETs and is therefore widely used to characterize SOI material. In order to characterize the SOI material, in particular with respect to their mobility, a simple model for the current through a MOSFET is employed: For small $V_{ds}$ the drain current $I_d$ increases linearly with drain voltage. In this so called linear regime of the output characteristics (i.e. $I_d$ versus drain-source voltage ($V_{ds}$) for
different gate voltages $V_{gs}$) the current is given by

$$I_d = f_g C_{ox} \frac{\mu}{1 + \theta(V_{gs} - V_{th})} \cdot (V_{gs} - V_{th}) V_{ds},$$  \hspace{1cm} (2)

Again, $C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{d_{ox}}$ is the gate oxide capacitance per unit area and $d_{ox}$ is the gate oxide thickness, i.e. buried oxide thickness. $V_{th}$ is the threshold voltage, i.e. the gate voltage where the device switches from the off- to the on-state and $f_g$ is a factor that accounts for the geometry of the device. The factor $\theta$ takes series resistances into account, and is considered independent of the gate voltage. Figure 2 (a) and (b) show the output and transfer characteristics of a MOSFET. An important figure of merit of a MOSFET in the on-state is the so-called transconductance $g_m$ giving the amount of drain current change with altering gate voltage:

$$g_m = \frac{\partial I_d(V_{ds} = \text{const.})}{\partial V_{gs}}$$ \hspace{1cm} (3)

![Figure 2: Schematic cross section (a), output (b) and transfer (c) characteristics of a MOSFET.](image)

The quality of the SOI material is reflected in the electronic transport properties of the material, i.e. in the effective carrier mobility $\mu$. In order to determine the mobility $\mu$ from the device characteristics we use the so-called $I_d/\sqrt{g_m}$-method which is particularly useful since it provides values for $\mu$ which are not influenced by parasitic series resistances. It is now easy to show that

$$\sqrt{f_g \mu C_{ox} V_{ds} (V_{gs} - V_{th})} = \frac{I_d}{\sqrt{g_m}}$$ \hspace{1cm} (4)

Therefore, measuring $I_d$ versus $V_{gs}$ at small drain-source bias (typically 0.05 to 0.1V), calculating $g_m$ and plotting $I_d/\sqrt{g_m}$ versus $V_{gs}$ yields a straight line. The
slope of this line is simply \( \sqrt{f_g \mu C_{ox} V_{ds}} \) from which the mobility \( \mu \) can be extracted provided that the geometry factor \( f_g \) is known. In rectangular MOSFETs \( f_g \) is the ratio of channel width and channel length \( f_g = W/L \). However, since in our experiment we deal with circular pseudo-MOSFETs the geometry factor is a little more complicated. Nevertheless, a closed expression for the ratio between width and length can be computed also in the circular case: 

\[
 f_g = \frac{2\pi}{\ln(R/r)} \]

where \( R, r \) are radii of the circular pseudo-MOSFET as shown in Fig. 5.

3 Device Fabrication

The fabrication of the devices will be carried out in the central clean room facility of the IMS. All participants have to wear a full cover with hoods, gowns and boots. The advisor will instruct the participants how to dress and how to behave in the clean room. Since the work will be done in the central facility great care has to be taken. In particular, contamination is a severe issue and therefore the participants have to wear gloves at all times when being in the clean room. Protective clothing such as apron, a second pair of gloves with sleeves and a face shield is mandatory when working with hazardous chemicals.

Each participant will get three SOI samples. In addition, a bulk silicon substrate will be cleaved and every participant will get as many dummy samples as needed. The fabrication procedure is listed below. During your lab-work, protocol the fabrication process and take as many notes as necessary since this will be attached to the written report as an appendix.

Mesa definition:

- a bulk silicon wafer is coated with HMDS and photoresist, pre-baked on a hot plate at 100°C for 45s and subsequently cleaved into 2x2 cm² pieces with a diamond scribe.
- remove the photoresist with acetone, rinse in propanol
- dehydration of the samples on a hot plate at 115°C for 5 minutes
- apply primer HMDS
- resist (AZ 1505) spin-on at 4200 rpm; pre-bake on a hot plate at 100°C for 45s
- 1st lithography with mask-aligner: expose the sample with 7mW/cm² for 15s
- develop for 30s (MIF:H₂O=1:1), rinse thoroughly in DI water
- post-exposure bake on hot plate at 100°C for 5 minutes
for mesa etching mix 50ml H$_2$O, 100ml HNO$_3$ and 5ml BOE (buffered oxide etch). Note the order of the chemicals!! Caution: BOE contains hydrofluoric acid (HF), an extremely hazardous chemical that can lead to severe injuries.

- determine the etch rate of the chemical solution by etching dummy samples for several different durations, remove the resist in acetone, rinse in propanol, blow dry with nitrogen and measure the etch depth with a surface profiler

- determine expected etch duration, etch the SOI sample until you see that all SOI is gone and rinse immediately afterwards in DI water

- remove the photoresist in acetone, rinse in propanol, blow dry

![Figure 3: Schematics of the mesa etch process.](image)

**Contact configuration 1**

- clean samples in Piranha

- remove the native oxide on the mesa (the circular mesa consists of SOI) of sample no. 1 with BOE, rinse for a few minutes and then immediately mount the sample into the sputter deposition tool.

- deposit 200nm Al.

- dehydration of sample no. 1 on a hot plate at 115°C for 5 minutes

- apply primer HMDS

- resist (AZ 1505) spin-on at 4200 rpm; pre-bake on a hot plate at 100°C for 45s

- 2nd lithography, expose as stated above

- develop for 30s (see above), rinse thoroughly in DI water

- post-exposure bake on hot plate at 100° for 5 minutes
• etch Al in PAN-etch
• remove resist in acetone, rinse in propanol and blow dry with nitrogen

Contact configuration 2

• dehydration of sample on a hot plate at 115°C for 5 minutes
• apply primer HMDS
• resist (AZ 5214) spin-on at 4200 rpm; pre-bake on a hot plate at 100°C for 45s
• 2nd lithography, image reversal process. Expose the samples for 10s followed by a post-exposure bake on the hot plate at 115°C for 90s; flood exposure for 20s.
• develop in undiluted developer for 30s, rinse thoroughly in DI water
• dip in BOE solution for 10s, rinse in DI water for 2 minutes, the samples are then mounted in an e-beam evaporation chamber and aluminum (200nm) is deposited.
• put the samples in acetone, lift-off aluminum, rinse in propanol and blow dry with nitrogen

Contact configuration 3

• samples will be cleaned in Piranha (sulfuric acid/hydrogen peroxide mixture) for 10min at 65°C. Rinse thoroughly in DI water, blow dry with nitrogen.
• mount the samples in PECVD tool, deposit 100nm SiO₂ at 300°C.
• dehydration of sample on a hot plate at 115°C for 5 minutes
• apply primer HMDS
• resist (AZ 1505) spin-on at 4200 rpm; pre-bake on a hot plate at 100°C for 45s
• 2nd lithography as in “contact configuration 1”.
• develop for 30s (see above), rinse thoroughly in DI water
• using BOE etch all SiO₂, rinse in DI water, blow dry
• remove resist in acetone, rinse in propanol, blow dry
- dip samples in BOE for 10s, rinse in DI water for 2 minutes, the samples are then mounted in the sputter tool and 100nm Ni is deposited.
- anneal samples in nitrogen atmosphere in an RTA at 500°C for 1 min
- etch away superficial Ni in Piranha (see above).

Figure 4: Schematics of the three different contact configurations.

Figure 5 shows a scanning electron microscopy image of a readily fabricated circular pseudo-MOSFET. The width and channel length of the device are shown as well. The buried oxide (BOX) serves as the actual gate oxide as already mentioned above.

4 Electrical Measurement and Characterization

Electrical measurements will be performed with an Hewlett Packard Semiconductor Parameter Analyser. The sample will be mounted in a probe station as
Figure 5: Microscope image of a fabricated pseudo MOSFET.

schematically shown in Fig. 6. The following measurements and characterizations should be made:

- Measure (all devices) the drain current versus gate voltage (transfer characteristics) over a large gate voltage range (e.g. ±40V) for drain voltages of up to 2V starting at 0.1V. Plot the transfer characteristics on a linear and a log-scale plot. Compare the on-currents, the leakage currents due to the ambipolar behavior and the inverse subthreshold slopes of the different devices.

- Measure (all devices) the output characteristics over the same drain and gate voltage range. Plot the output characteristics.

- Extract the mobility of the fabricated samples using the $\frac{I_d}{\sqrt{g_m}}$-method. Plot the mobility versus the channel length of the different devices.

5 Writing your Report

After the characterization you are supposed to write a short report. Since writing reports is often considered as being boring you should write it with the following background:

After finishing your BSc/MSc degree at TU Dortmund University you work for an up-and-coming consulting company in the semiconductor industry. Your speciality is the implementation of new materials into existing CMOS production lines and you have been called by the CTO (chief technical officer) - one of your
friends - of a foundry that has been producing logic ICs with conventional doped source/drain contacts. The CEO (chief executive officer) of the foundry has only a limited technical background but has to decide between several technology options. To improve the performance of the company’s ICs he wants to move ahead to the next CMOS generation by scaling down the device dimensions. The CTO calculated that moving to the next generation by scaling would not pay-off since the devices would suffer from SCE so severely that they cannot be used for logic circuits anymore. He argues that the company has to move from bulk to SOI substrates which, however, implies a severe financial investment into new fabrication tools.

The CTO discusses her findings with the CEO who is absolutely not amused and tells your friend that he recently read in the PM! magazine that the mobility in SOI is worse than in bulk and moving to SOI technology would not pay-off since the financial investments would be too cost-intensive. Your friend agrees but replies that the investments are necessary in order to keep-up with the company’s competitors and that SOI is the way to go. The CTO is worried that the CEO will ruin the company with launching a new product that will eventually exhibit a worse performance than its predecessors. On the other hand, she just bought a house and desperately needs this job. So, she decides to hire you to perform a technical study on SOI MOSFETs. You should convince the CEO of going for SOI technology in the following way:

- Write a cover letter stating your recommendation, the key benefits of using SOI technology. Point out to the enclosed material that backs up your recommendation (the technical annex which contains the results of your experimental work). Remember that the CEO has only a limited technical background - he understands dollars not MOSFETs. Therefore, the style of the letter should be a mixture of business- and technical-like. But most of all it should be convincing! You want to help your friend keeping her job.
You might want to use this opportunity to give your consulting company a fancy name.)!

- Prepare a technical annex. In this annex you should explain and discuss the pseudo-MOSFET results. You should also state and explain shortly the method you used to obtain the mobility data and the experimental procedure. To this annex your lab notes should be added. Refer to these notes in the technical annex.

The report can either be written in German or English.

**Bibliography**


1: R=3350µm, r=300µm
2: R=2900µm, r=300µm
3: R=2900µm, r=790µm
4: R=975µm, r=100µm
5: R=975µm, r=287µm
6: R=850µm, r=300µm
7: R=1280µm, r=300µm
8: R=1800µm, r=790µm
9: R=1800µm, r=200µm
10: R=975µm, r=195µm
11: R=3350µm, r=270µm
12: R=2900µm, r=300µm
13: R=2900µm, r=790µm